

Amendments to the Claims:

This Listing of Claims will replace all prior versions and listings of claims in the Application:

1 1. (Currently Amended) A semiconductor device comprising:

2 a substrate;

3 a gate region on top of the substrate;

4 a ~~first and second~~ sidewall liner ~~liners~~ situated on a ~~first and second sides~~ side of
5 the gate region ~~respectively, the first and second sidewall liners~~ and having a vertical
6 part contacting a sidewall ~~sidewalls~~ of the gate region and a horizontal part contacting
7 the substrate; and

8 a ~~first and second~~ recessed ~~spacers~~ spacer situated on top of the ~~first and~~
9 ~~second~~ sidewall ~~liners respectively~~ liner,

10 wherein a height of the ~~first and second~~ recessed ~~spacers~~ spacer is lower than a
11 height of the sidewall liner, and

12 wherein the horizontal part of each the sidewall liner is shorter than the
13 corresponding recessed spacer on top thereof; and

14 a contact etch stopping (CES) layer formed over the recessed spacer and having
15 a predetermined stress level being one of compressive and tensile.

1 2. (Original) The device of claim 1 wherein the height of the recessed spacer
2 is at least 50 Å lower than the height of the vertical part of the sidewall liner.

1 3. (Currently Amended) The device of claim 1 wherein the horizontal part of
2 each gate sidewall liner is at least 10 Å shorter than the recessed spacer ~~spacers~~.

1 4. (Original) The device of claim 1 wherein the gate region further includes a
2 gate dielectric and electrode layers.

1 5. (Original) The device of claim 4 wherein the height of the gate region does
2 not exceed 1800Å.

1 6. (Original) The device of claim 1 wherein the recessed spacer is SiN
2 based.

1 7. (Original) The device of claim 1 wherein the recessed spacer further
2 includes Ge, Ar, or O₂ based impurities.

1 8. (Original) The device of claim 1 wherein the sidewall liner is oxide based.

1 9. (Cancelled)

1 10. (Currently Amended) The device of claim [[9]] 1 wherein the CES layer
2 imposes a compressive stress.

1 11. (Currently Amended) The device of claim [[9]] 1 wherein the CES layer
2 imposes a tensile stress.

1 12. (Currently Amended) The device of claim [[9]] 1 wherein the stress level of
2 contact etching stopper layer is larger than 200M Pa.

1 13. (Original) The device of claim 9 wherein the thickness of the CES layer is
2 smaller than 600Å.

1 14. (Withdrawn - Currently Amended) A method for fabricating at least one
2 semiconductor device having a gate region and recessed spacers, comprising:

3 forming a substrate;

4 forming a gate region on top of the substrate, the gate region having a gate
5 electrode and a gate dielectric region;

6 forming ~~two~~ a sidewall liner along a side of ~~liners~~ liners ~~confining~~ the gate region
7 ~~therebetween~~;

8 forming ~~a two-spacers~~ spacer on top of the sidewall ~~liners~~ liner ~~on both sides of~~
9 ~~the gate region~~, a height of the ~~spacers~~ spacer matching substantially a height of the
10 sidewall ~~spacers~~ liner;

11 reducing the width of the sidewall ~~liners~~ liner underneath the ~~spacers~~ spacer to
12 pull back from an edge of each spacer by a predetermined distance; and

13 forming ~~two~~ a recessed ~~spacers~~ spacer by reducing the height of the formed
14 ~~spacers~~ spacer, wherein the reduced spacer height reduces device channel stress.

1 15. (Withdrawn - Currently Amended) The method of claim 14 wherein the
2 forming ~~two-spacers~~ a spacer further includes depositing spacer material and etching
3 the deposited spacer material so that the top of the spacer slopes ~~spacers~~ ~~slope~~ down
4 from the top of the sidewall ~~liners~~ liner to a horizontal part of the sidewall liner that
5 extends along the substrate from the gate region.

1 16. (Withdrawn - Currently Amended) The method of claim 14 wherein the
2 reducing further includes:

3 forming an oxide layer over the spacer ~~spacers~~, the sidewall liner ~~liners~~, and the
4 gate region;

5 etching the oxide off within a predetermined time period so that the width of the
6 sidewall liner is ~~liners are~~ pulled back for a predetermined distance.

1 17. (Withdrawn - Currently Amended) The method of claim 14 wherein
2 forming ~~two~~ the recessed spacer ~~spacers~~ further includes selectively etching the
3 ~~spacers~~ spacer to reduce at least 50Å in the height of the spacer ~~spacers~~ to form the
4 recessed spacer ~~spacers~~.

1 18. (Withdrawn - Currently Amended) The method of claim 14 further
2 comprising introducing one or more impurities to the ~~spacers~~ spacer to further reduce
3 the device channel stress.

1 19. (Withdrawn - Currently Amended) The method of claim 14 wherein the
2 predetermined distance pulled back from the edge of ~~each~~ the spacer is at least 10Å.

1 20. (Withdrawn - Currently Amended) The method of claim 14 further
2 comprising forming a contact etch stopper (CES) layer over the recessed spacer
3 ~~spacers~~ for further modifying the device channel stress.

1 21. (Withdrawn) The method of claim 20 wherein the CES layer imposes a
2 compressive stress.

1 22. (Withdrawn) The method of claim 20 wherein the CES layer imposes a
2 tensile stress.

1 23. (Withdrawn - Currently Amended) A transistor comprising:
2 a substrate;
3 a gate electrode on top of the substrate;
4 ~~a first and second~~ an "L" shaped gate sidewall ~~liners~~ confining liner along the
5 gate electrode and therebetween, ~~the first and second sidewall liners~~ having a vertical
6 part contacting sidewalls a sidewall of the gate electrode and a horizontal part
7 contacting the substrate; and
8 ~~a first and second recessed~~ spacer ~~spacers~~ situated on top of the ~~first and~~
9 ~~second~~ sidewall liner ~~liners~~ respectively; and
10 a contact etching stopper (CES) layer situated over the recessed spacer ~~spacers~~,
11 wherein a height of the spacer ~~first and second spacers~~ is lower than a height of
12 the gate sidewall liner ~~liners~~ and a width of the gate sidewall liner ~~liners~~ is shorter than
13 that of the spacer ~~first and second spacers~~, and
14 wherein the recessed ~~spacers~~ spacer is doped with predetermined impurities
15 for modifying a channel stress of the transistor.

1 24. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the
2 recessed ~~spacers~~ spacer is at least 50 Å lower than the gate sidewall liner ~~liners~~.

1 25. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the
2 gate sidewall ~~liners~~ liner is at least 10Å shorter than the recessed spacer ~~spacers~~.

1 26. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the
2 impurities doped into the recessed spacer ~~spacers~~ includes Ge, Ar, or O₂ based
3 impurities.

1 27. (Withdrawn - Currently Amended) The transistor of claim 23 wherein the
2 CES layer formed over the recessed spacers is thicker than the recessed spacer
3 ~~spacers~~.

1 28. (Withdrawn) The transistor of claim 23 wherein the contact etching stopper
2 layer is thinner than 600Å.

1 29. (Withdrawn) The transistor of claim 23 wherein the contact etching stopper
2 layer imposes a tensile stress less than 1.5G Pa.

1 30. (Withdrawn) The transistor of claim 23 wherein the contract etching
2 stopper layer imposes a compressive stress less than 1.0G Pa.

1 31. (Withdrawn - Currently Amended) A semiconductor device comprising:
2 a substrate;
3 a gate region on top of the substrate;
4 ~~two a~~ a sidewall liners liner situated on at least one of two sides of the gate region;
5 and
6 a spacer situated on top of each sidewall liner,
7 a contact etching stopper layer over each spacer ~~the spacers~~,

8 wherein the contact etching stopper layer is thicker than each the spacer.

1 32. (Withdrawn) The device of claim 31 wherein the thickness of contact
2 etching stopper layer is smaller than 600Å.

1 33. (Withdrawn) The device of claim 31 wherein the contact etching stopper
2 layer imposes tensile stress.

1 34. (Withdrawn) The device of claim 33 wherein a stress level of the contact
2 etching stopper layer is less than 1.5G Pa.

1 35. (Withdrawn) The device of claim 31 wherein the contact etching stopper
2 layer imposes compressive stress.

1 36. (Withdrawn) The device of claim 35 wherein a stress level of the contact
2 etching stopper layer is less than 1.0G Pa.

1 37. (Withdrawn - Currently Amended) A semiconductor device comprising:

2 a substrate;

3 a gate region on top of the substrate;

4 two an "L" shaped sidewall liner ~~liners situated on~~ contacting each of two
5 opposed ~~[[sides]]~~ sidewalls of the gate region;

6 a recessed spacer situated on top of each sidewall liner; and

7 a contact etching stopper layer formed over the spacers, the ~~sidewall~~ sidewalls,
8 and the gate region,

9 wherein the contact etching stopper layer is thicker than the spacer, and

10 wherein the sidewall liner is higher and wider than the recessed spacer.

1 38. (Withdrawn) The device of claim 37 wherein the thickness of the contact
2 etching stopper layer is smaller than 600Å.

1 39. (Withdrawn) The device of claim 37 wherein the contact etching stopper
2 layer imposes a tensile stress.

1 40. (Withdrawn) The device of claim 39 wherein a stress imposed by the
2 contact etching stopper layer is less than 1.5G Pa.

1 41. (Withdrawn) The device of claim 37 wherein the contact etching stopper
2 layer imposes a compressive stress.

1 42. (Withdrawn) The device of claim 41 wherein a stress imposed by the
2 contact etching stopper layer is less than 1.0G Pa.